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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,061	12/11/2003	Wing K. Luk	YOR920030136US1 (8728-621)	1252
46069	7590	10/16/2006		EXAMINER
F. CHAU & ASSOCIATES, LLC 130 WOODBURY ROAD WOODBURY, NY 11797			BERNSTEIN, ALLISON	
			ART UNIT	PAPER NUMBER
				2824

DATE MAILED: 10/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/735,061	LUK ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Allison Bernstein	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 09 August 2006.  
 2a) This action is FINAL.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-53 is/are pending in the application.  
 4a) Of the above claim(s) 11-53 is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-10 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 11 December 2003 is/are: a) accepted or b) objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date _____.	6) <input checked="" type="checkbox"/> Other: <u>search history</u> .

## **DETAILED ACTION**

Claims 1-53 are pending in the application. Claims 11-53 are withdrawn from consideration.

### ***Election/Restrictions***

Claims 52-53 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 10 March 2006.

Applicant's election with traverse of Species 1, claims 1-10, in the reply filed on 9 August 2006 is acknowledged. The traversal is on the ground(s) that there is no serious burden on Examiner to simultaneously prosecute all claims of Species 1-9. This is not found persuasive because there is currently no generic claim pending in the case. In order for a generic claim to exist it must be generic to all claims. The multiple independent and distinct species would indeed constitute a burdensome search. Each of the mutually exclusive characteristics identified in the restriction requirement, dated 7 July 2006, makes the required search complex, and would therefore represent an undue burden on the Examiner to simultaneously prosecute all claims for species 1-9.

The requirement is still deemed proper and is therefore made FINAL.

Claims 11-51 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected species, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 9 August 2006.

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Leung et al. (US 6,468,855).**
3. **Regarding claim 1,** Leung et al. disclose a gated diode memory cell comprising: at least one transistor (301 in figure 3A); and a gated diode (302 in figure 3A) in signal communication with the at least one transistor.
4. **Regarding claim 2,** Leung et al. disclose a gated diode memory cell as defined in claim 1 wherein a first terminal of the gated diode (302 in figure 3A) forms one terminal of a storage cell and a second terminal of the gated diode forms another terminal of the storage cell (column 6 liens 25-30).
5. **Regarding claim 3,** Leung et al. disclose a gated diode memory cell as defined in claim 2 wherein the gate of the gated diode (302 in figure 3A, see also figure 4B) is

implemented in the form of a shallow trench (60 in figure 4B, see also column 8 lines 30-35).

6. **Regarding claim 4,** Leung et al. disclose a gated diode memory cell as defined in claim 3, the gate of the gated diode (302 in figure 3A, see also figure 4B) comprising a poly trench (60 in figure 4B) surrounded by thin oxide (46 in figure 4B, see also column 7 lines 46-48) with silicon (for example 41 in figure 4B) disposed underneath and surrounding the thin oxide (46 in figure 4B).

7. **Regarding claim 5,** Leung et al. disclose a gated diode memory cell as defined in claim 4 wherein the poly trench is cylindrical (60 in figure 4B and column 10 lines 20-25).

8. **Regarding claim 6,** Leung et al. disclose a gated diode memory cell as defined in claim 4, the gate of the gated diode (302 in figure 3A) comprising a metal oxide semiconductor ("MOS") capacitor (column 7 lines 56-57).

9. **Regarding claim 7,** Leung et al. disclose a gated diode memory cell as defined in claim 2 wherein the gate of the gated diode (302 in figure 3A, see also figures 3B-E) is planar (313 in figure 3E).

10. **Regarding claim 8,** Leung et al. disclose a gated diode memory cell as defined in claim 7 wherein the gate of the gated diode (302 in figures 3A-3C, see also 313 in figure 3E) is disposed above a diffusion area (between 312 and 314 in figure 3E).

11. **Regarding claim 9,** Leung et al. disclose a gated diode memory cell as defined in claim 8, further comprising an oxide layer (308 in figure 3E) disposed between the

gate (313 in figure 3E) of the gated diode and the diffusion area (between 312 and 314 in figure 3E).

12. **Regarding claim 10,** Leung et al. disclose a gated diode memory cell as defined in claim 7, the gated diode comprising a planar metal oxide semiconductor ("MOS") capacitor (313 in figure 3E and column 7 lines 56-57).

### ***Conclusion***

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Hazani (US 5,278,785) is cited to teach a gated diode structure. Chan (US 4,370,737), Oowaki et al. (US 5,307,315), Wojciechowski (US 5,841,703), Bill et al. (US 6,134,146), and Foss et al. (US 6,980,448) are cited to teach transistors configured as diodes.

When responding to this office action, applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner in locating appropriate paragraphs.

A shortened statutory period for response to this action is set to expire three months and zero days from the date of this letter. Failure to respond within the period for response will cause this application to become abandoned (see MPEP 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Allison Bernstein whose telephone number is 571-272-9011. The examiner can normally be reached on Monday-Friday 7AM-4PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AB

  
**VAN THU NGUYEN**  
**PRIMARY EXAMINER**